FUTURE UNIVERSITY IN EGYPT جامعة المستقبل

Faculty of Engineering & Technology

Integrated Circuits Technology

Information :

Course Code :	ELE 525	**Level :**	Undergraduate	**Course Hours :**	3.00- Hours

Department : Specialization of Electronics & Communication

Area Of Study :

Improve student's foundational background, theories and mechanism of the state-of-the art of integrated circuit technology.
Develop the student skills in modeling of the interconnect parameters, layout design, and the design rules for integrated circuit technology.
Improve students understanding of the link between the circuit design and the layout design by introducing design parameters, performance parameters, CAD models, etc.

Description :

Defining terms, Technology roadmap, Basic silicon processes, Fabrication of passive and active components, Process integration and standard technologies, Process simulation, Layout design rules, Layout parasitics, Typical examples, Layout techniques, Interconnect modeling, Substrate coupling issues, ESD protection.

Course outcomes :

a.Knowledge and Understanding: :	
1 -	State the basic definitions and terminologies of the state-of-the art of integrated circuit technology
2 -	Explain methods of silicon processes and fabrication; wafer formation, photolithography, well and channel formation, silicon dioxide (SiO2), isolation, gate oxide, gate and source/drain formations, contacts and metallization, and passivation.
3 -	Define the layout design rules including well rules, transistor rules, contact rules, metal rules, via rules, micron design rules, and MOSIS scalable design rules.
4 -	Estimate the modeling of the interconnect parameters; wire geometry, interconnect modelling, capacitance, resistance, and inductance, skin effect, interconnect impact, delay, energy, crosstalk, inductive effects, and an aside on effective resistance and Elmore delay, interconnect engineering, and logical effort with wires.
b.Intellectual Skills: :	
1 -	Develop layout models for electronic circuits applied on the integrated circuit technology;
2 -	Use electronic circuit layout models for circuit simulation;
3 -	Use the interconnect parameters to evaluate circuit performance.
c.Professional and Practical Skills: :	
1 -	Build electronic circuits for a specific application using related layout software tools;
2 -	Develop technical report writing skills.
d.General and Transferable Skills: :	
1 -	Collaborate effectively within multidisciplinary team

2 -	Communicate effectively.
3 -	Effectively manage tasks, time, and resources.
4 -	Search for information and engage in life-long self-learning discipline.

Course Topic And Contents :

Topic	No. of hours	Lecture	Tutorial / Practical
Basic definitions and terminologies.	5	3	2
Silicon processes and fabrication. Wafer formation.	5	3	2
Photolithography. Well and channel formation. Silicon dioxide (SiO2), and isolation. Gate oxide, gate and source/drain formations. Contacts, metallization, and passivation.	10	6	4
Layout design rules for: well, transistor, contact, metal, via, and micron design.	10	6	4
MOSIS scalable design rules.	10	6	4
Modeling of the interconnect parameters: wire geometry, interconnect modelling, capacitance, resistance, inductance, skin effect, and interconnect impact.	10	6	4
Delay, energy, and crosstalk.	10	6	4
Elmore delay.	5	3	2
Logical effort with wires.	5	3	2
Layout parasitics ESD protection.	5	3	2

Teaching And Learning Methodologies :

Interactive Lecture
Discussion
Problem Solving
Experimental Learning
Cooperative Learning
Research
Presentation
Site Visit (Guided Field Trip)

Course Assessment :

Methods of assessment	Relative weight %	Week No	Assess What
Mid- Exam I 15 Mid- Exam II	15.00		
Assignments/project	10.00		
Final Exam	40.00		
Lab Experiment	5.00		
Mid- Exam I	15.00		
Oral Exam	5.00		
Quizzes	10.00		

Recommended books :

): Neil H.E. Weste and David Harris; "CMOS VLSI
Design, A Circuits and Systems Perspective", 4rd Ed.; Pearson Addison-Wesley;
2011.
Jan M. Rabaey; ñDigital Integrated Circuitsò, 2nd Ed.; Prentice Hall;
2003.