Efficient FPGA implementation of FFT/IFFT Processor

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Abstract

ð The Fast Fourier Transform (FFT) and its inverse (IFFT) are very important algorithms in signal processing, software-defined radio, and the most promising modulation technique; Orthogonal Frequency Division Multiplexing (OFDM). This paper explains the implementation of radix-2
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single-path delay feedback pipelined FFT/IFFT processor. This attractive architecture has the same multiplicative complexity as radix-4 algorithm, but retains the simple butterfly structure of radix-2 algorithm. The implementation was made on a Field Programmable Gate Array (FPGA) because it can achieve higher computing speed than digital signal processors, and also can achieve cost effectively ASIC-like performance with lower development time, and risks. The processor has been developed using hardware description language VHDL on an Xilinx xc5vsx35t and simulated up to 465MHz and exhibited execution time of 0.135εS for transformation length 256-point. This results show that the processor achieves higher throughput and lower area and latency.

INTERNATIONAL JOURNAL OF CIRCUITS, SYSTEMS AND SIGNAL PROCESSING 2009, January