

FPGA implementation of Radix-22 Pipelined FFT Processor

AHMED SAEED ABDELSAMEA SAYED , Mohamed E. Elbably, Gamal Abd-Elfadeel, Mohamed I. Eladawy

Abstract

The Fast Fourier Transform (FFT) is very important algorithm in signal processing, softwaredefined radio, and wireless communication. This paper explains the realization of radix-2

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single-path delay feedback pipelined FFT processor. This architecture has the same multiplicative complexity as radix-4 algorithm, but retains the simple butterfly structure of radix-2 algorithm. The implementation was made on a Field Programmable Gate Array (FPGA) because it can achieve higher computing speed than digital signal processors (DSPs), and also can achieve cost effectively ASIC-like performance with lower development time, and risks. The processor has been developed using hardware description language VHDL and simulated up to 465 MHz on an Xilinx xc5vsx35t for transformation length 256-point.

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