

Implementation of Low-Power Multiply-Accumulate (MAC) Unit for IoT Processors

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Abstract

Embedded processors are key building blocks for IoT platforms. Multiply-Accumulate (MAC) units are vital arithmetic circuits in several applications performed by the processors including digital signal processing (DSP). It is necessary to reduce the power consumed by the processor. In this paper, the design and implementation of 32-bit MAC unit optimized for low-power budget targeting IoT processors is introduced. The proposed MAC unit is capable of performing several 16bit, dual 16-bit, and 32-bit MAC operations that can be carried out on signed and unsigned numbers with up to three operands involved. The performance of MAC unit is analyzed in terms of delay and power. The unit is described in VHDL, implemented and simulated on Vivado and tested using Nexys 4 DDR board featuring Xilinx's Artix-7 FPGA.

*2nd European Conference on Electrical Engineering and Computer Science
GGEU'423:+. "Dgtp."423:0 2018, December